BlueICe

Your ideas into Silicon

Company overview

Q3-2013

Partnering with the Customer

- Partnership based on **TRANSPARENCY, ACCOUNTABILITY** and **FLEXIBILITY**

- Team of **PROFESSIONALS** of the semiconductor industry offering a unique combination of **COMPETENCES**, and >150 man-year **EXPERIENCE** in the development of **ASICs** and world-class **ASSPs**

Management Commitment and Principles

- **EFFICIENCY**
  - Silicon development is very expensive
  - Good choices in architecture, "technologies" used, development, verification, validation methodology make a big difference in terms of development cost
  - Unique expertise in this area
- **QUALITY**
  - Covering the complete development process
  - Covering the end product

Management Commitment and Principles

- **TRANSPARENCY**
  - Full transparency on status, plans, resources, processes
- **FLEXIBLE&AGILE**
  - adapting to customers needs and processes
  - Fast to commit
- **ACCOUNTABLE**
  - Willing to share project and business risk
- **LIFETIME SUPPORT**
  - Beyond the life of the product

Value

- Turnkey solutions
  - Hardware/software co-design track record
  - Ultra low power design technology
- Privileged partnerships with silicon vendors
- More than 150myears of design and project management expertise
- State of the art performance
  - Proven
  - Design methodology
- Broad application and market expertise

History - Status

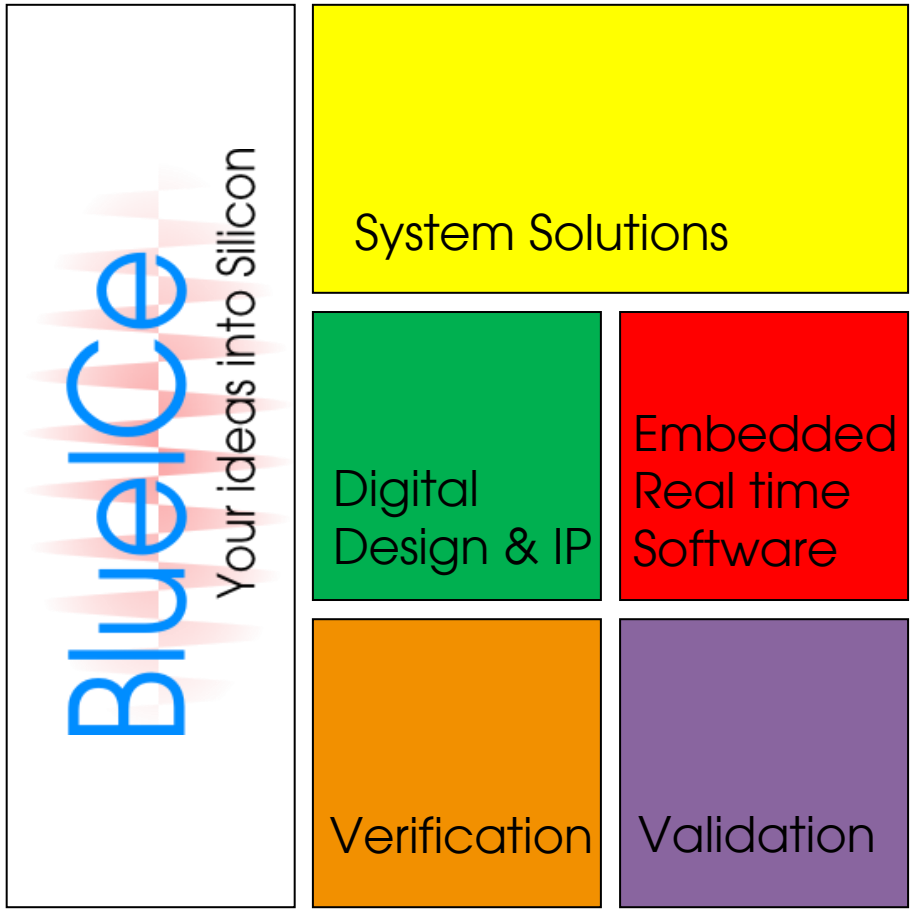
- Founded 2010 by Henri Cloetens and Leon Cloetens
- 13 persons at BlueICe (direct and indirect)
  - Analog/digital/software architecture, digital design, real time software, FGPA-validation
  - Most in R&D
- Moved into new premises, Molenstraat 19, Zaventem at the end of 2012
  - Equipped a complete validation LAB

The founders

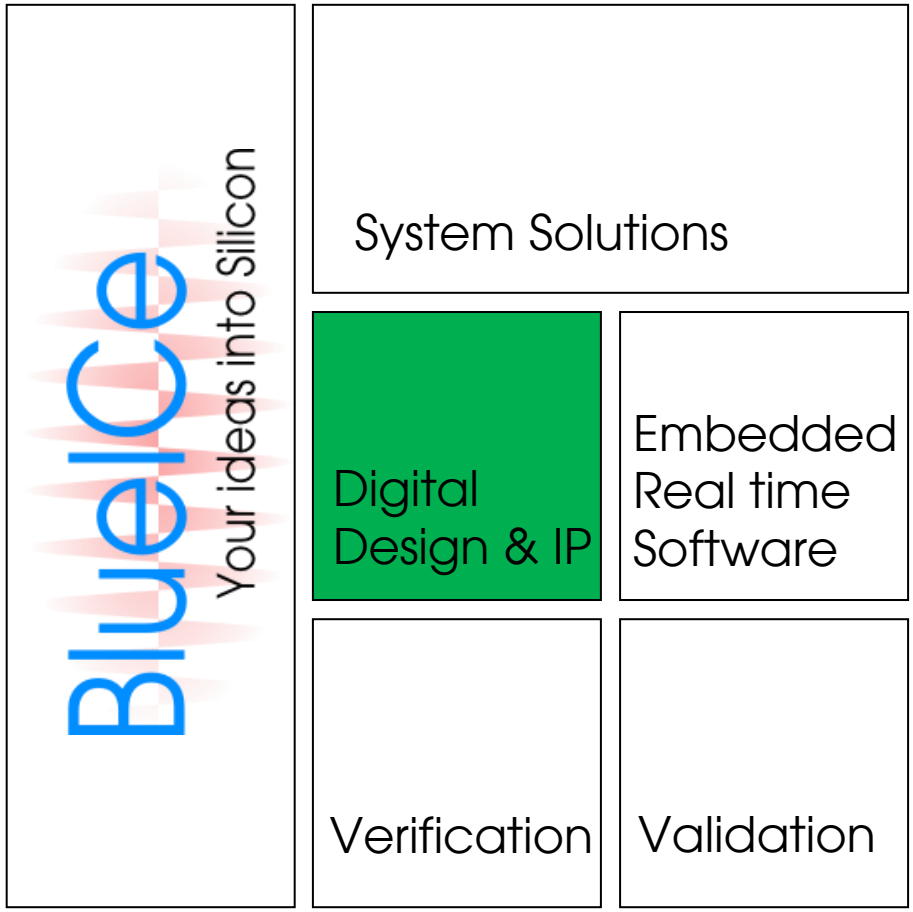
- Henri Cloetens - CTO
  - MSEE degree at the Catholic University of Leuven Belgium
  - > 25 years track record in the semiconductor industry at Philips, now NXP and Freescale
  - Designed world first CD/DVD front end SOC, which achieved more than 50% market share
  - Senior system architect at Motorola Semiconductor
  - H/W & S/W; System Architected the Coldfire Digital Audio MCU's
  - Developed complete RADAR baseband solutions for automotive based on Power architecture

- Leon Cloetens - CEO
  - MSEE Electronics at the Catholic University of Leuven Belgium
  - > 25 years track record in the semiconductor industry
  - 15 years of R&D experience at Alcatel, Alcatel-Micro
  - 10 years of General Management at Alcatel-Micro, ST-Micro and ST-Ericsson
  - Responsible for Bluetooth, GPS, Wireless LAN product portfolio
  - Managed large R&D teams and complex projects (>100my, multisite)
  - SOC in deep submicron down to 40nm

Product offer



Design Consultancy and IP



Design Consultancy and IP

- Our prime focus is to turn your ideas into Silicon
- Our core competence is System architecture, digital architecture, digital design, embedded software and verification
  - With a focus on ultra low power solutions
- One stop shop, taking ownership of large or smaller projects
- Not afraid to share development and business risk
- Our commitment is to be flexible, fast, committing, with quick feedback cycles.
  - We typically offer free feasibility studies

Design Consultancy and IP

- BlueICe is investing in own IP-blocks and tools
  - Invested in a number of easy to adapt RTL blocks
    - E.g. interfaces as SPI, JTAG, …
  - Invested in a number of breakthrough low power architectures: processor, and a digital PLL architecture

- BlueICe's business model is based on excellent execution not on binding its customers through IP rights

Area's of expertise – where algorithm meets (digital) architecture

Area	Description - proofpoints
Modulators/Demodulators	Developed modulator/demodulator solutions for several wireless standards. This is about merging algorithmic design with detailed digital micro-architecture, necessary to obtain performance and low power consumption
Coders	Large expertise on coder design: Reed Solomon, Vitterbi, BCH. Developed a BCH coder with 32bit error correction capability, a Vitterbi coder with constraint length of 9 bit, leveraging deep understanding of coder algorithms with detailed digital micro-architecture.
Packet processing	Developed a generic packet coprocessor core, 'managed' by a low clock speed 32bit controller. The core can manage packet processing independent for most of the time, cutting processor load and power consumption. Furthermore the core is 'memory-less', allowing the supplies to be cut between transfers. It has been demonstrated on a Bluetooth implementation, consuming less than .3mA in active mode in a 90nm TSMC reference process.
Memory controllers	Developed multiport DRAM controllers, applicable in very high throughput requirement environments. This controller achieved in a 5port configuration in a typical usage example [mixing display, processor etc… traffic] 70% of the maximum memory throughput
Processor based design	Did designs based on market available processors: Cortex Mx technology from ARM. Coldfire technology from Freescale.
Ultra low power	Micro architecture reducing per function clock to the minimum need; clock gating functions deep in the hierarchy; only allowing clock when state change is required. Furthermore implemented complex supply gating schemes.

IP portfolio

Category	IP	Description
Interfaces	SPI	SPI interface capable to run up to 50Mhz in a 90nm reference TSMC platform. Optionally it can be used in a packet transfer friendly mode, allowing it to communicate with a central memory without the need of Host interaction or DMA control.
	JTAG/SWD	JTAG/SWD interface
Microcontroller peripherals	Bus arbiters	Arbiter technology optimizing the power consumption on a controller bus by only allowing clock and data on the processor bus when transfer is needed. Contains multi master options, eliminating the need for a DMA in the system.
	Watchdog, timers etc…	A number of AMBA compatible peripherals.
BLUSP Signal Processor		BlueICe proprietary DSP architecture with significant controller capabilities/
modulator/demodulator	OQPSK modulator/demodulator	OQPSK modulator which in conjuntion with a Vitterbi decoder achieves close to Shannon limit performance. It allows for a datarate up to 1Mbit/s in the 868Mhz unlicensed spectrum
coder/decoder	Vitterbi coder/decoder	Vitterbi coder with constraint length of 9 bit, leveraging deep understanding of coder algorithms with detailed digital micro-architecture.

Tool competences and strategy

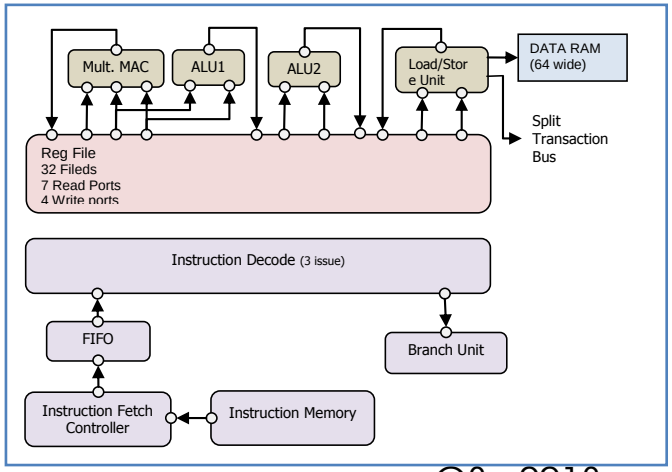
- Used a wide variety of industry standard tools
  - Cadence
  - Synopsys
  - Mentor
- Are capable and did design both in VHDL and Verilog
- Verification based on Verilog, System Verilog
  - With heavy use of C-based randomized patterns
  - Verified for a wireless solution the complete software stack with the hardware implementation prior to silicon availability

Ultra Low Power Technology

- Ultra low power is the focal point in all BlueICe's IP
- Strategy is to push an architecture till most (90%) of its potential is realized and going further starts "to really hurt"
  - Each function – deep in the hierarchy – is clocked at lowest possible speed
  - Clock is gated to a function only when state change is required
- Mastering complex multi-supply designs
- Architecture and micro architecture
  - E.g. BLUSP architecture can run up to 800Mhz in 40nm, which conversely means at very low voltage it still has significant performance and ultra low power

Processor, Embedded Software and DSP Expert

- Developed a novel ultra low power processor architecture: BLUSP
- Complete tool chain based on an external compiler (developed by a TU-Delft spinoff: BlueBee)
- Capable to modulate/demodulate wireless standards with a `medium' data rate of up to few Mbit/s data rate
  - 802.11.n/.ah, 802.15.4(g)



BluSP Processor(1)

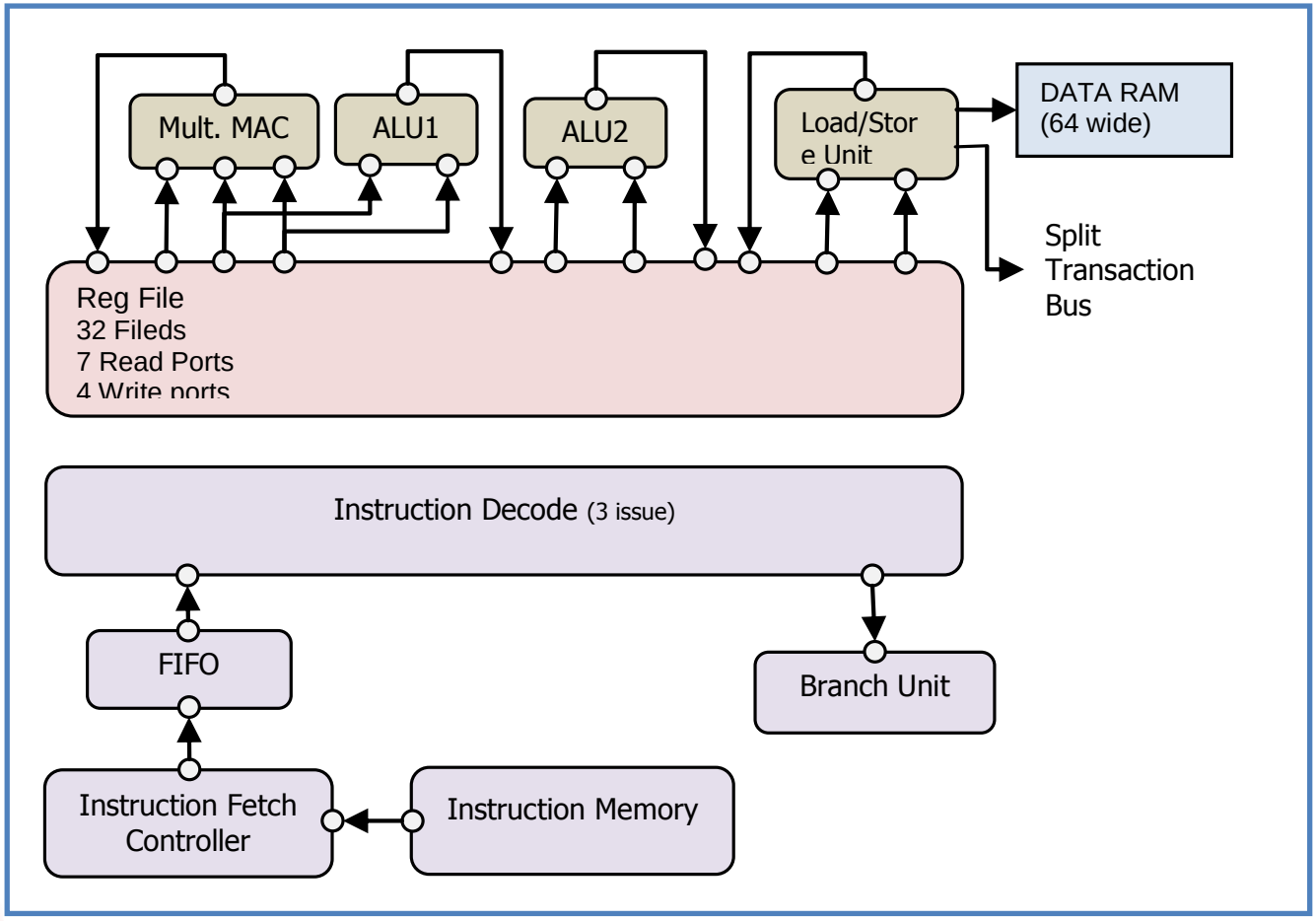
HIGH PERFORMANCE ARCHITECTURE	- BluSP is a high performance DSC (mix of DSP and Controller) core. - **3 Issue** core architecture - Single cycle complex MAC **- 600 Mhz** speed in a 40nm LP library
WIRELESS applications	- Its calculation power and speed make it fit to implement also complex and high data rate modulation applications - It can e.g. handle a **256 point FFT** in **1350 cycles** with 16bit precision
Audio processing	- Its 32 bit capability make it fit to handle audio applications - The core can implement in 32bit an **MP3** decoder, running at **4Mhz clock rate**

BluSP Processor(2)

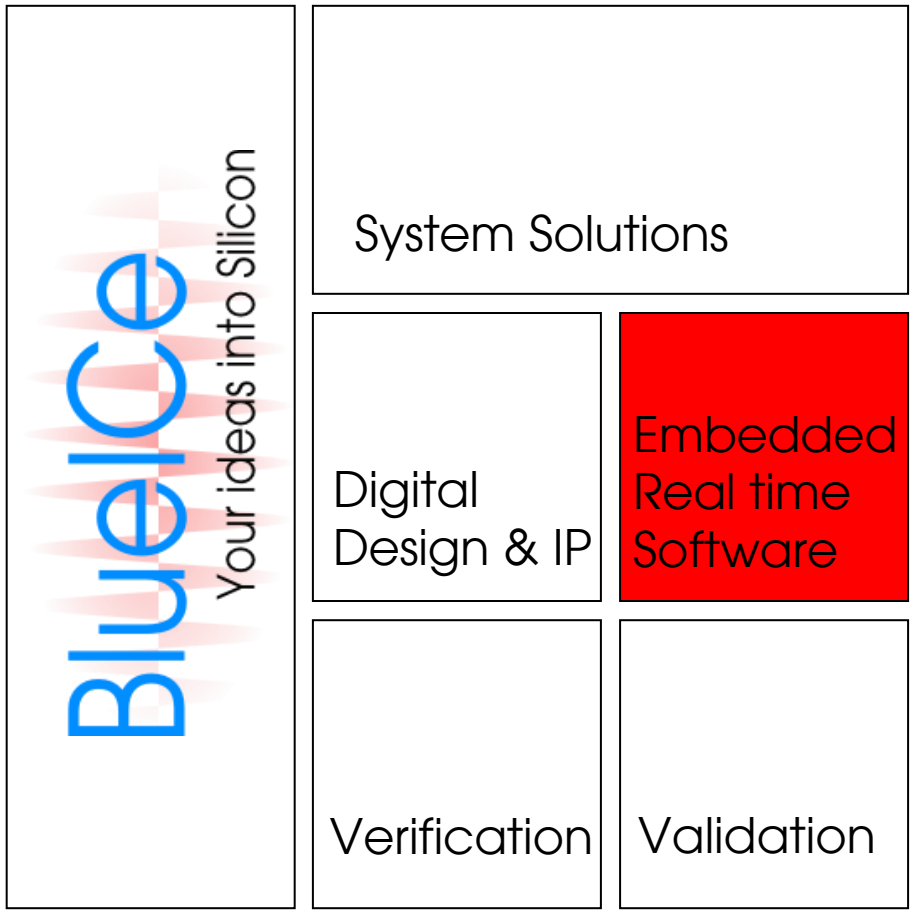
Ultra low power	- The core consumes in a **40nm LP** TSMC library, operated at 1.1Volts a current of **13uA/Mhz** with a typical program. It consumes 21uA/Mhz with a "smoker" pattern. This pattern is loading the slots and the complex MAC at 100% - These data are based on simulations with **post layout** extraction of load capacitances and resistances
Software Development Kit	**ECLIPS based** software development kit Small, ultra RISC, instruction set with few (only one) specific data type -> makes it **very easy** to optimize **standard C code** for the core Comprised of a (assembly) code simulator, debugger, profiler, compiler. Developed in cooperation with an external partner.

BLUSP processor

- Communication processor architecture advancing the state-of-the-art by a factor of 3 or more.



Embedded Real time software



Expertise

- More than 50% of the R&D done in BluelCe was around embedded software development
  - Packet processing
  - Communication protocols: e.g. complete Bluetooth stack (linklayer, host layer, profiles)
- Deep real time knowledge
  - Design mixing assembler, C
  - Specified and evaluated/optimized compiler for the BLUSP architecture

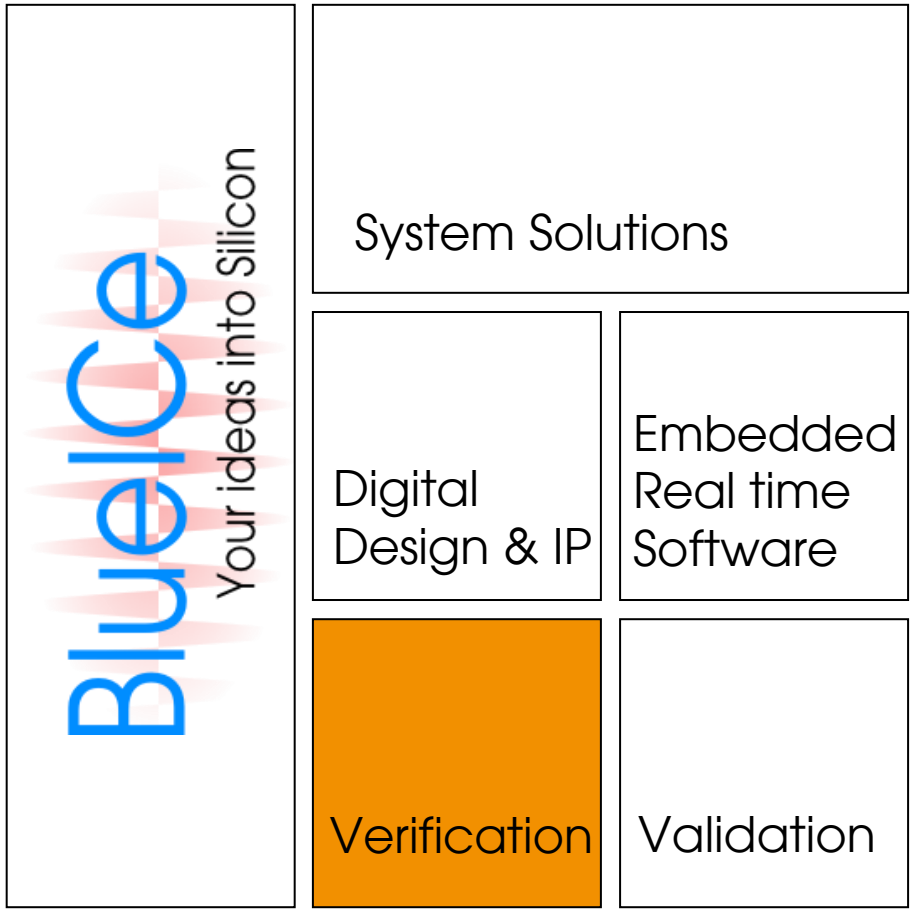
Expertise

- Implemented heavily constrained problems
  - Real time, time budget limited
  - Memory limited
  - Complex memory systems, combining, FLASH, ROM, EEPROM, SRAM, patching hardware
- Development done in a simulation based environment
- Development based on on target hardware

Expertise

- Development expertise on
  - ARM based architecture: M0 and M3
  - BLUSP architecture
  - Freescale proprietary architectures
- Languages
  - C
  - Assembly
  - touched C++
  - PYTHON

Verification



verification

- Vision
  - Simulation based verification is the cornerstone in building a complex multi technology product
    - It avoids iterations
    - It is less expensive than FPGA verification
    - Well done it is more covering than end product validation
    - When a system surpasses a certain complexity limit it can be not sufficient any more

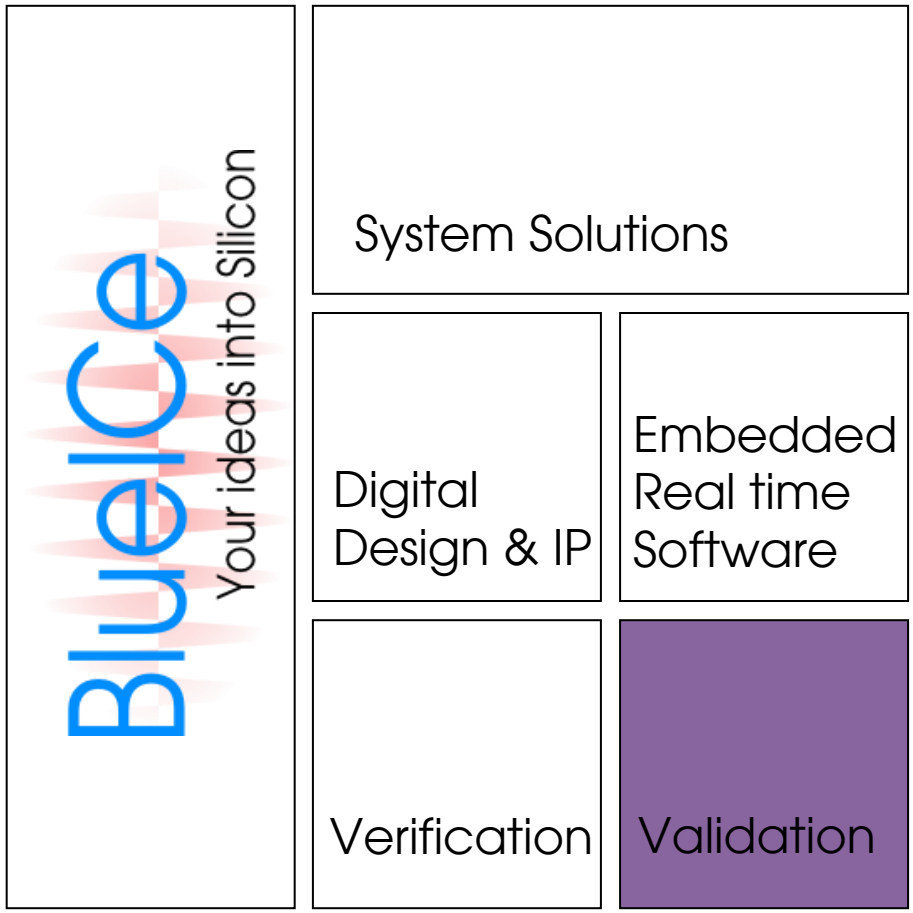
verification

- FPGA based verification
  - FPGA based verification can be a plus when complexity is high
  - When it allows to "field trial" the application = building real life verification scenario's is very difficult or impossible
- In what BluelCe did sofar, simulation based verification was applied successfully resulting in:
  - great solution quality
  - allowing to capture in simulation several system errors

verification

- Coverage is increased by
  - Combining hardware with models of analog, RF
  - With models of the outside world (e.g. air interface)
  - Simulating hardware with the complete software solution
  - Simulation the system together with externally captured real life signals
- Further increased by randomizing patterns
- Verification is based on:
  - C-based patterns
  - Linked into the verification environment through PLI interface

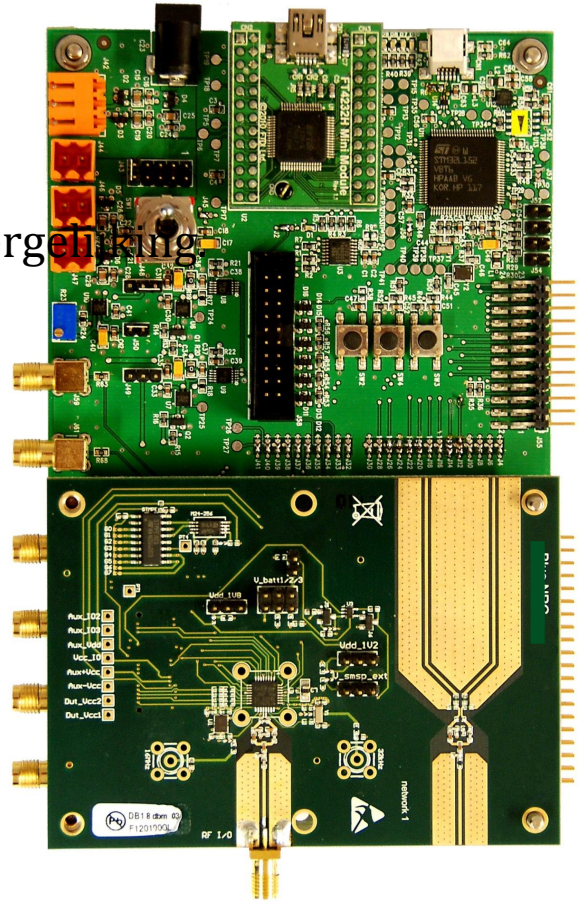
Design Consultancy and IP



Validation and FPGA

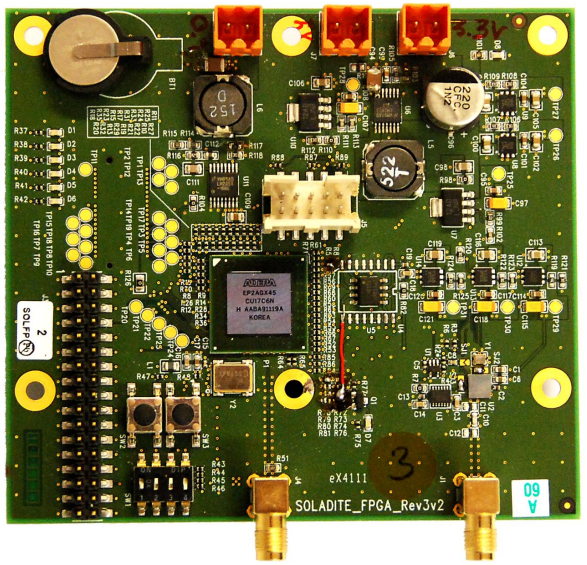
- Validation is a complex and time consuming part of IC or FPGA development
- BlueICe offers its Validation expertise and IP as a separate service.
- In our toolbox: FPGA based generic characterization boards, PC based automated validation sequences, GUI…
- Expertise and top notch engineering team

Typ hier uw vergelijking



FPGA

- Digital SOC development and FPGA development are similar in terms of competence
- FPGA development as a pre-silicon validation vehicle and standalone development
- Expertise with Xilinx and Altera families and tools
- Expertise with processor on FPGA
- Expertise with encrypted FPGA



FPGA and Validation Services Offer(1)

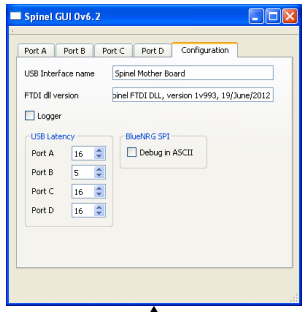
- Offer separate FPGA, Validation and test Services
- Hardware:
  - Reuse big part of the hardware in the different steps: reconfiguration of the functionalities (FPGA), daughter/mother board splitting.
- Software:
  - Interfaces with the hardware. Drivers to communicate with the boards.
  - Graphical control interfaces (GUIs).
  - Automated test (ATE). Control of the boards and test instruments. Generation of reports.

FPGA and Validation Services Offer(2)

- Benefits
  - Open Source
  - Professional and Affordable philosophy
  - Offer is based on an experienced team and on past work

Validation Platform

GUI



python
Automatic test Script (Phyton based)

Front End

Connector

Ext Connector

Main Board / FPGA

FPGA

Digital

Com

Test Block

SPI

UART

Channel 3

Channel 4

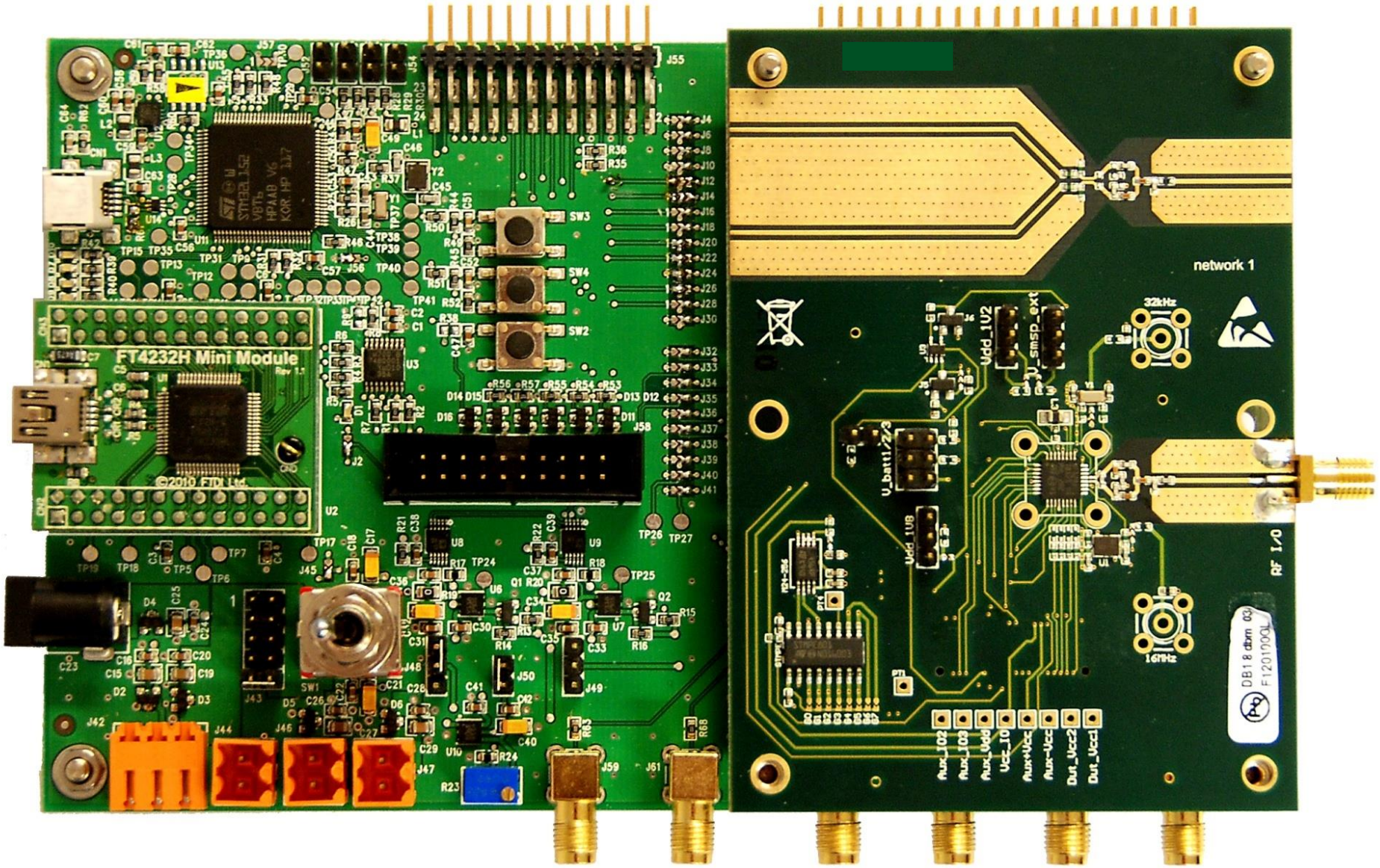
USB Bridge

PMU

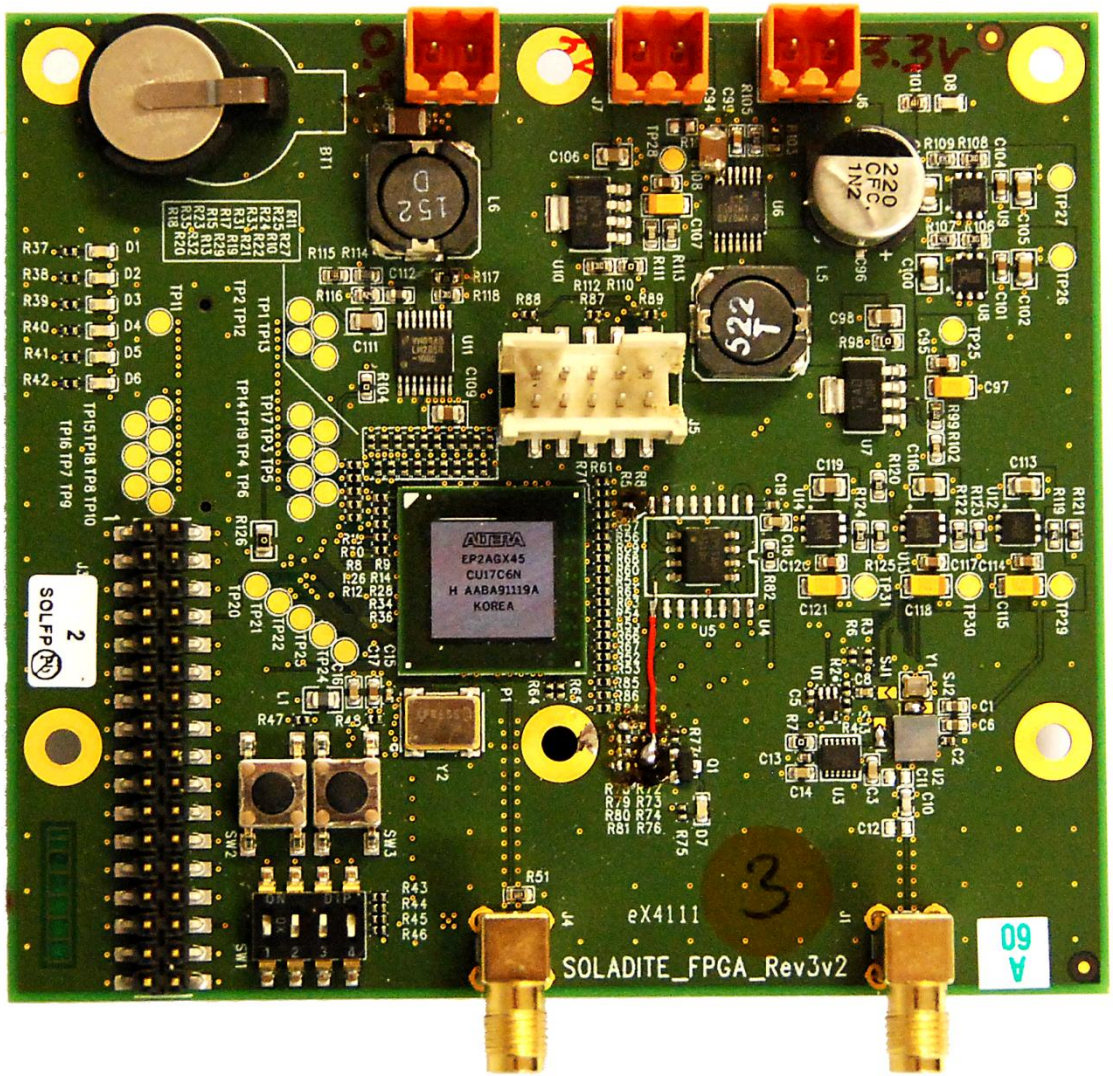
DLL
(C Based)

USB

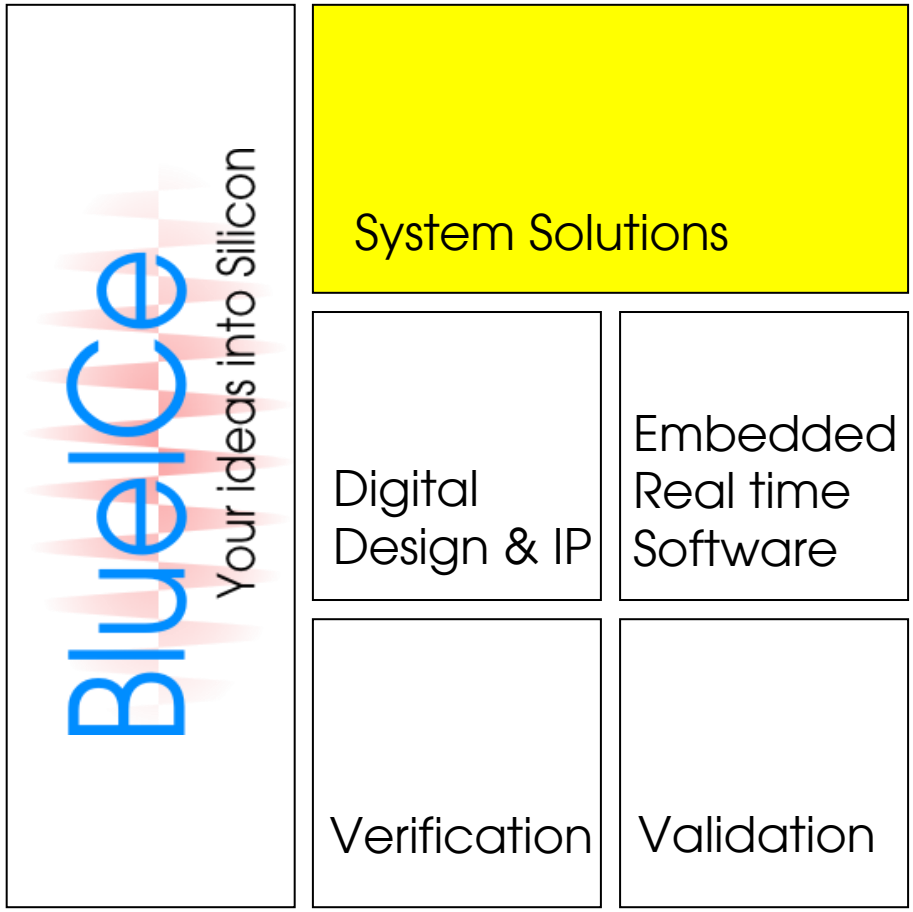
Example of an evaluation environment



FPGA platform



Product offer



Wireless System Architecture Expert

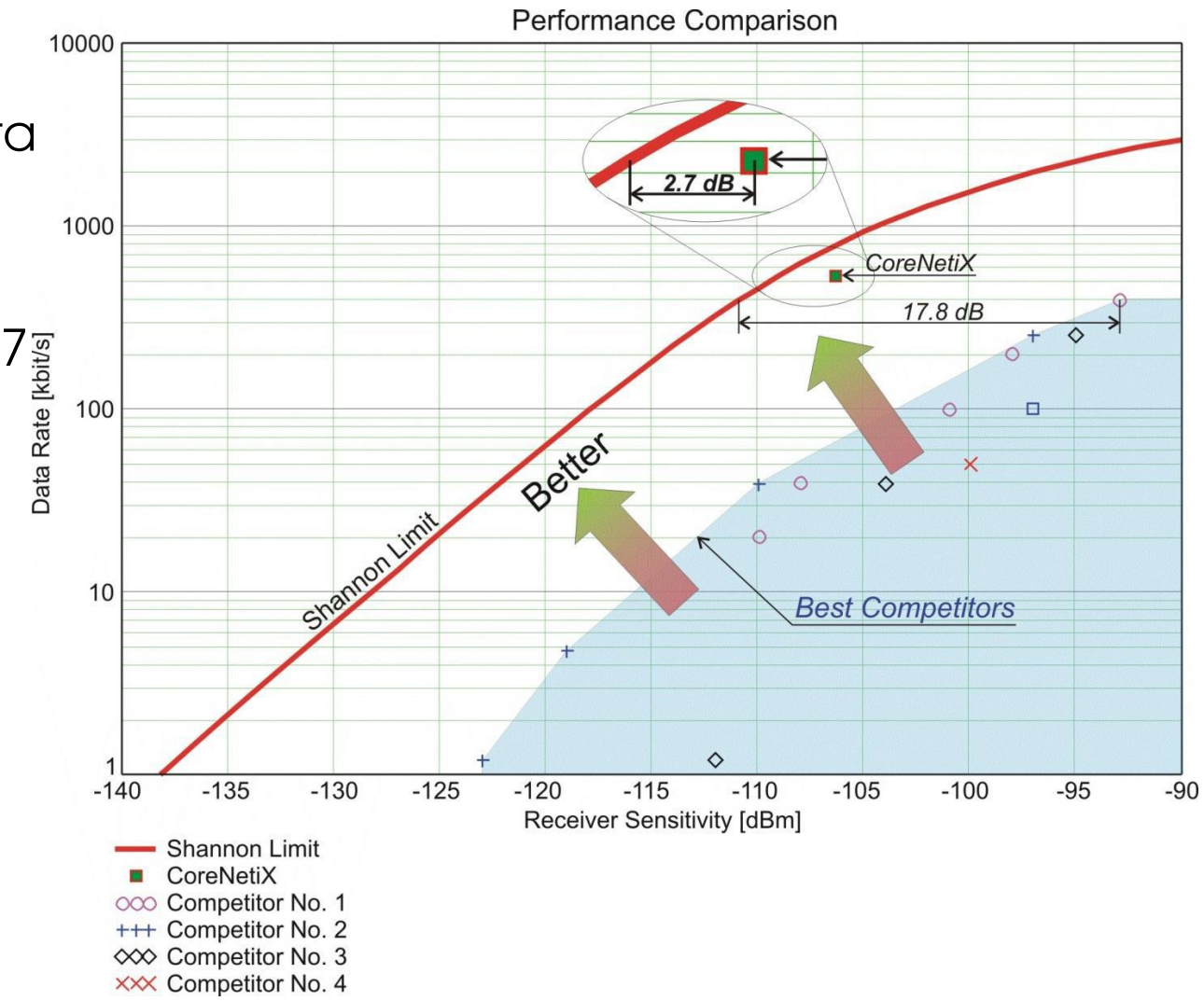
- Developed from ground up a complete short range radio SOC.
  - With external RF/Analog design solution
  - Silicon, link layer, application layers
  - Full validation and qualification done by BlueICe
  - From ground up: all knowledge is residing in BlueICe
  - Kernel of the IC is (generic) packet processor controlled by a control processor

Wireless System Architecture Expert

- Developed modulation technology for an industrial wireless standard: 2db away from the Shannon limit
- We invested in a well equipped lab allowing us to extensive testing, including e.g. temperature tests
- We invested over the last 2years ~450kE in our own (wireless) technology (processor, PLL)

Modulator/demodulator example: leveraging the co-competence of algorithm and micro-architecture

- Demonstrated the core with a (CoreNetiX) High Data Rate solution
- Offers extraordinary performance: only 2.7 dB worse than theoretical limit.
- Leveraging the processor and the coprocessor of the complete solution



Turnkey SOC Development

- All competences in house to develop a complete (digital) SOC.
- If RF or analog is required we cooperate with external RF or analog design houses
- If required prototyping, production test,… can be organized
  - E.g. we have an agreement in place with IMEC services giving us access to all TSMC technology/libraries/prototyping services
- All competences in house to validate, qualify

Bluetooth

- We developed turnkey a complete LE Bluetooth chip with an RF partner
  - SOC, Linklayer, Host, Profiles, Master mode, Slave mode
  - Development, validation and certification.
- We "used" several industry solutions, both LE only and mixed LE – full Bluetooth
  - Nordic, TI, ST-Ericsson
- Our host stack has been used into 2 architectures: Host stack on the companion processor and host on the LE device.
- We developed complete validation environment: validation board (SOC, M3-based application processor, PC – over USB – interface – sensor interface)

Solutions for Bluetooth

- BlueICe is capable to do a complete pre-certification validation
  - equipped lab
  - Including RF pre-qualification
  - BlueICe worked multiple times with AT4wireless in Spain to obtain Bluetooth certification
- BlueICe is participating in Bluetooth SIG
  - Participating systematically in interop events

Proofpoints

Proofpoints (1)

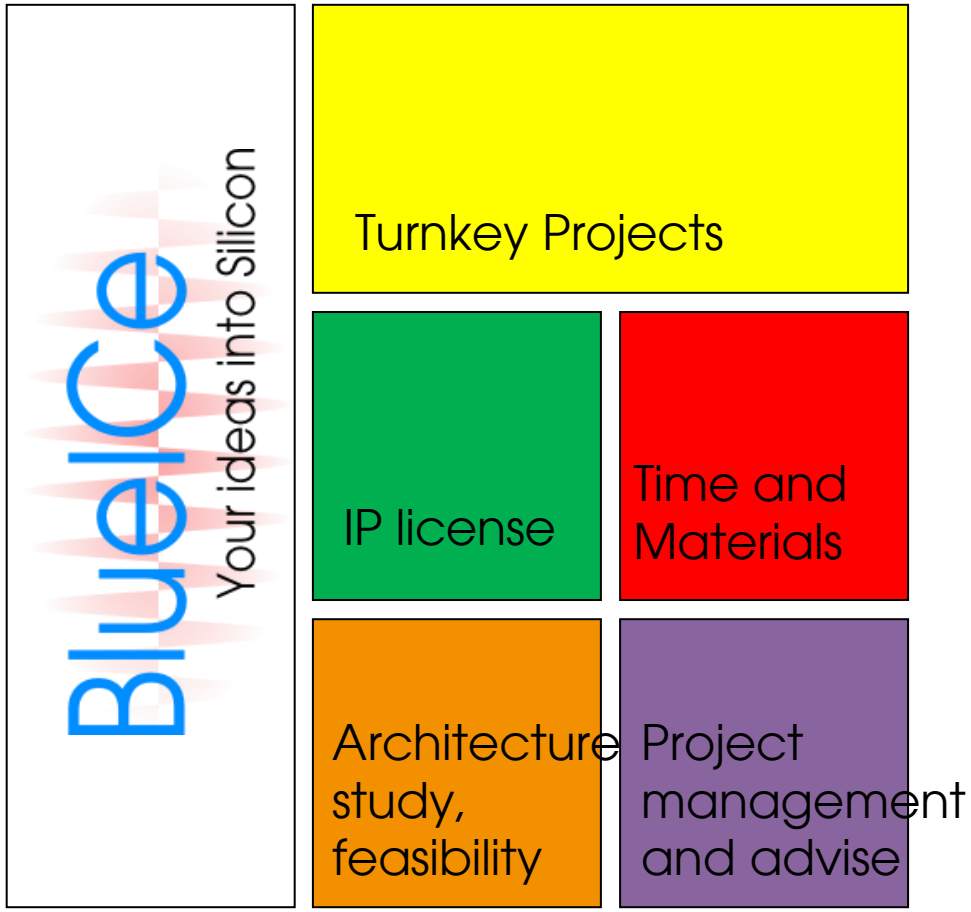
SHORT RANGE RADIO SOC (2011-2012)	Develop **from scratch** a short range radio SOC, in cooperation with an external RF partner – In production
INDUSTRIAL WIRELESS TECHNOLOGY (2012)	Developing from scratch an industrial network SOC, with an external RF partner. Developed the (proprietary) modulator and demodulator.
DSC IP (2012)	Developed from scratch a **high calculation** mix DSP, Controller Core targeted at low power – wireless – applications.

Proofpoints (2)

R&D partnerships	Partnership in place with academia on our **processing** and short range wireless technology. Part of this R&I is funded with public funds. (TUDelft and IMEC-INTEC Ghent) Partnership in place on **compilation technology** with Bluebee, a spinoff of TU-Delft (2012) Partnership in place with Allgo (Bangalore), developing part of our embedded software (2011) Signed access to TSMC library and TSMC prototype services agreement, With IMEC Services. Covers also "affordable" **processing** through MPW and MLR service. (2012) Partnership in place with **RF design** companies which are complementing our skill mix in wireless SOC development

Business Models

Business Models



Business Models

- Turnkey projects
  - SOC design
  - FPGA design
  - Validation
  - Embedded software
  - Willing to share business risk
- Time and Materials
- Architectural study
  - Feasibility study

Business Models

- IP license
  - Compensation based on License fee and royalty
- Project management, advise in general
  - In the area of Micro-electronics
  - E.g. on technical choices
  - E.g. on partner choices

Thank You